The Future of Analog IC Technology

MP6519

2.5V - 28V, 5A, H-Bridge Current Regulator

DESCRIPTION

The MP6519 is a monolithic, step-down, current-source driver for applications that require accurate and fast current-response control. The MP6519 achieves up to 5A of output current with excellent load and line regulation over a wide input supply range.

The four integrated MOSFET H-bridge control provide a fast dynamic load response and an ultra-high efficiency solution. For ease of use, the output polarity can be controlled by pulling MODE high or low.

By setting the full-scale output current through an external resistor, the output current can be dimmed by the PWM input signal from 0 - 100% of the full-scale current range.

Full protection features include load open, load-short protection, over-current protection (OCP), over-temperature protection (OTP), and input over-voltage protection (OVP). The MP6519 is available in a QFN-19 (3mmx3mm) package.

FEATURES

- Wide 2.5V to 28V Operating Input Range
- Up to 5A Output Load Current
- ± 2% Accuracy at Full-Scale Reference
- 65mΩ $R_{DS(ON)}$ for Each MOSFET of H-Bridge
- 100% Duty Cycle Operation of H-Bridge
- 30kHz to 300kHz Programmable Switching Frequency
- 20kHz - 100kHz PWM Input for Current Regulation
- Programmable Full-Scale Current
- Up to 94% Efficiency
- Selectable Current Polarity Mode
- Switching Auto-Disabled by PWM Input Detection
- 1μA Shutdown Mode
- Inherent Open-Load Protection
- Cycle-by-Cycle Over-Current Protection (OCP)
- Output Short-Circuit Protection (SCP)
- Input Over-Voltage Protection (OVP)
- Over-Temperature Shutdown
- Available in a QFN-19 (3mmx3mm) Package

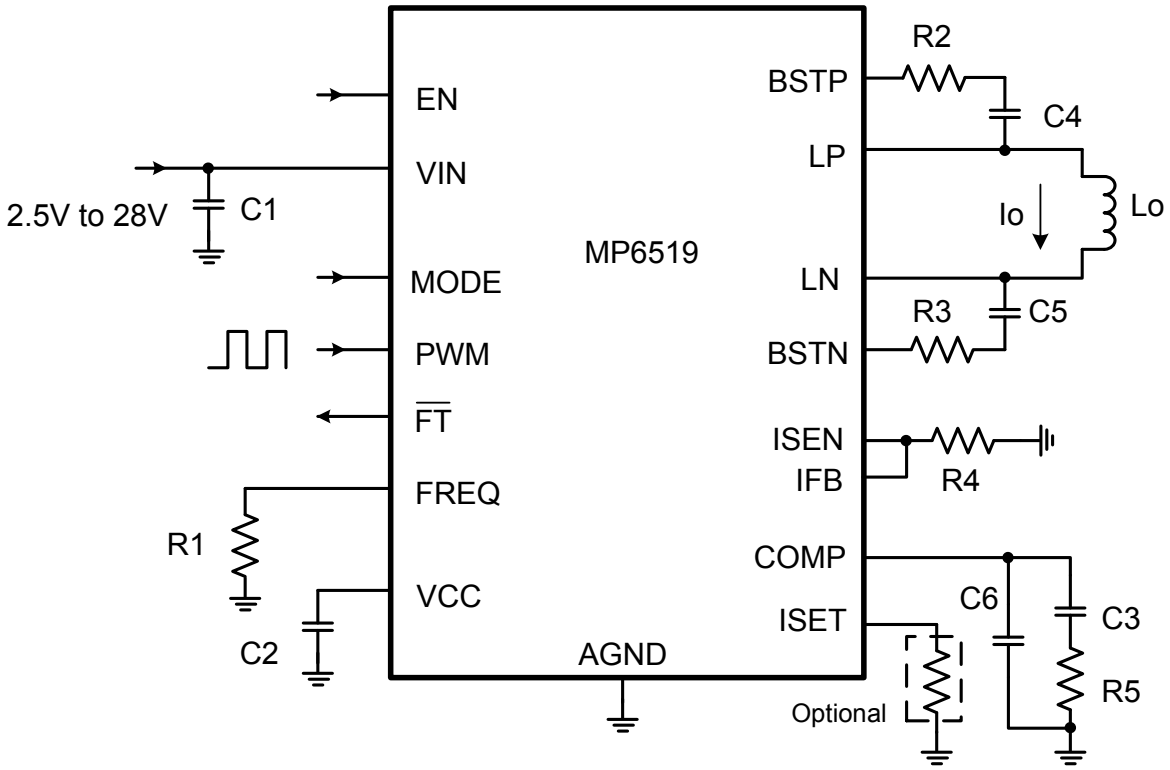
APPLICATIONS

- Current Regulators
- DC Motors
- Solenoid/Actuators

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6519GQ	QFN-19 (3mmx3mm)	See Below

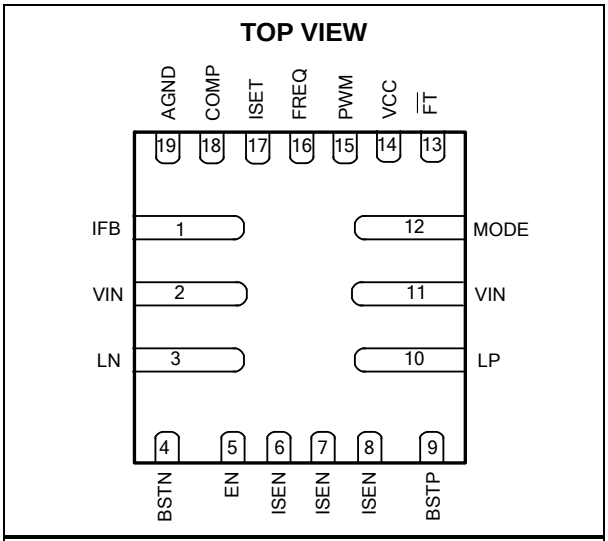
* For Tape & Reel, add suffix –Z (e.g. MP6519GQ–Z)

TOP MARKING

$\overline{\text{ARUY}}$
LLL

ARU: Product code of MP6519GQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-19 (3mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 35V
V_{LP}, V_{LN} ..... -0.3V to V_{IN} + 0.3V
V_{BSTP} ..... V_{LP} + 6V
V_{BSTN} ..... V_{LN} + 6V
All other pins ..... -0.3V to +6V
Continuous power dissipation (T_A = +25°C) (2)
QFN-19 (3mmx3mm) 2.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.5V to 28V
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
QFN-19 (3mmx3mm)	50	8	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

VIN = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
VIN operating range	V_{IN}		2.5		28	V
Turn-on threshold	V_{IN_ON}	VIN rising edge		2.3	2.45	V
Turn-on hysteretic voltage	V_{IN_HY}			0.15		V
IC Supply						
Shutdown current	I_{IN_SD}	EN = low			1	µA
Quiescent current	I_{IN_SBY}	Standby mode		370	450	µA
VCC regulator voltage	V_{VCC}	VIN > 5.2V	4.5	5	5.5	V
VCC regulator drop output voltage		VIN < 5V, 20mA load		100		mV
Logic						
EN high threshold	V_{EN_High}				1.5	V
EN low threshold	V_{EN_Low}		0.4			V
MODE input high threshold	V_{EN_High}				1.5	V
MODE input low threshold	V_{EN_Low}		0.4			V
PWM high threshold	V_{PWM_High}				1.5	V
PWM low threshold	V_{PWM_Low}		0.4			V
IC start-up delay	T_{delay}	EN active to switching		230	350	µs
Switching Frequency						
Switching frequency	fs	R_{FREQ} = 75kΩ	255	300	345	kHz
		R_{FREQ} = 750kΩ	22	30	38	kHz
Current Reference						
Current reference accuracy	V_{REF_FB}	V_{REF_FB} = 200mV	196	200	204	mV
		V_{REF_FB} = 50mV	47	50	53	mV
Loop Compensation						
Transconductance	G_{EA}			270		µA/V
Max source current				50		µA
Max sink current				50		µA
Power MOSFET						
High-side MOSFET on resistance			42	65	93	mΩ
Low-side MOSFET on resistance			42	65	93	mΩ
Minimum on time				200		ns
Bootstrap for High-Side Driver						
Forward voltage for BST charge				0.5		V
BST UVLO		Rising edge		2		V

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ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Protection						
Hiccup over-current threshold		R_{ISET} float	255	300	345	mV
Load short hiccup recovery timer				1		ms
Latch-off over-current threshold		R_{ISET} float, R_{SEN} = 40mΩ		13		A
Input over-voltage threshold	V_{INOVP}		28.2	30	31	V
Thermal shutdown (5)				150		°C
Thermal shutdown hysteresis				20		°C

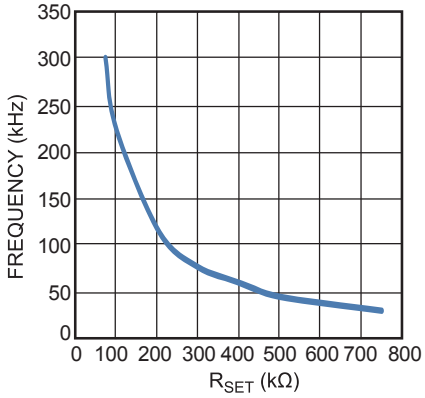
NOTE:

5) Guaranteed by design.

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TYPICAL PERFORMANCE CHARACTERISTICS

Switching Frequency vs. R_{SET}

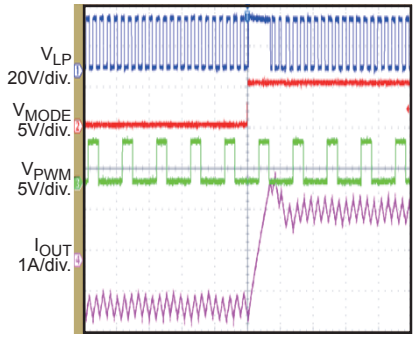


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Mode Transfer

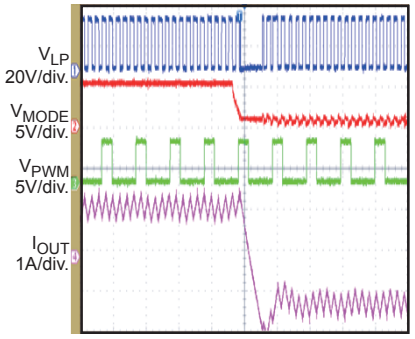
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE Low to High, 1Ω+100μH Load



20μs/div.

Mode Transfer

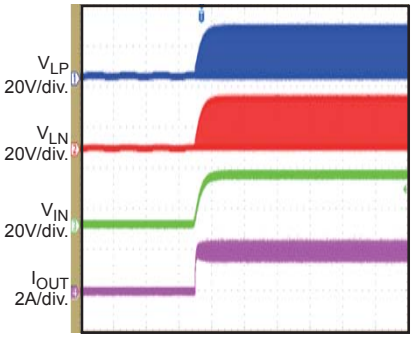
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE High to Low, 1Ω+100μH Load



20μs/div.

VIN Start-Up

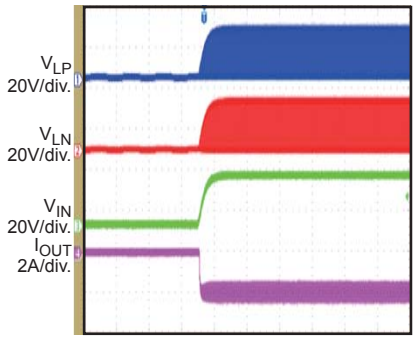
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load



20ms/div.

VIN Start-Up

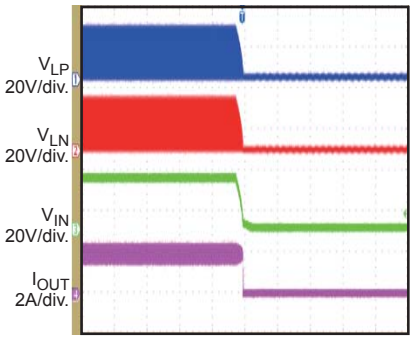
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



20ms/div.

VIN Shutdown

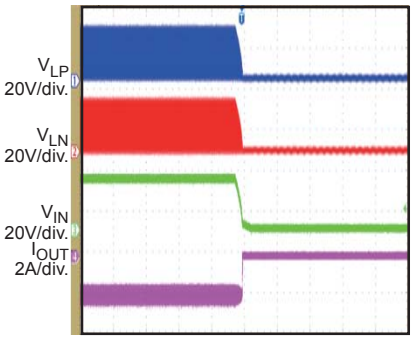
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load



100ms/div.

VIN Shutdown

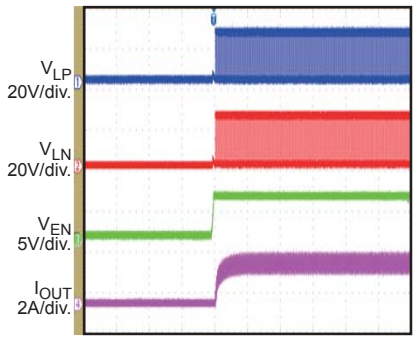
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



100ms/div.

EN Start-Up

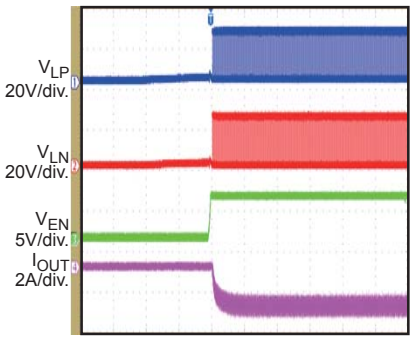
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load



2ms/div.

EN Start-Up

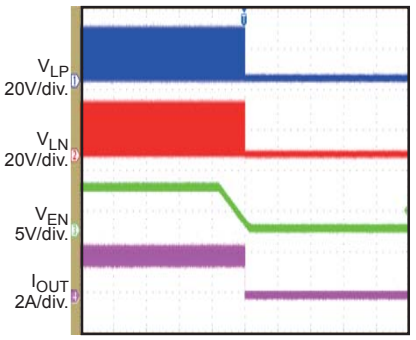
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



2ms/div.

EN Shutdown

V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load

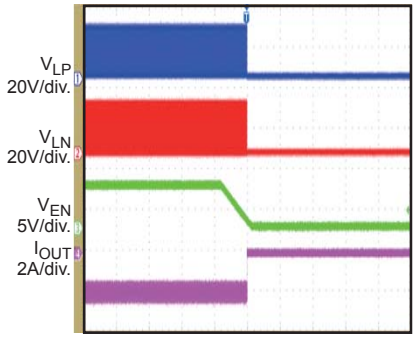


40ms/div.

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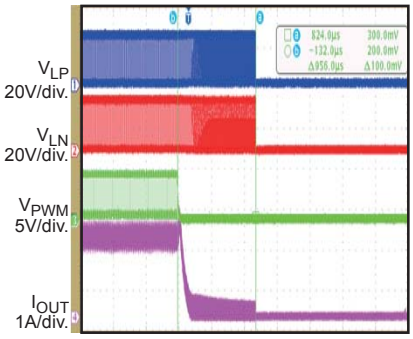
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

EN Shutdown
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



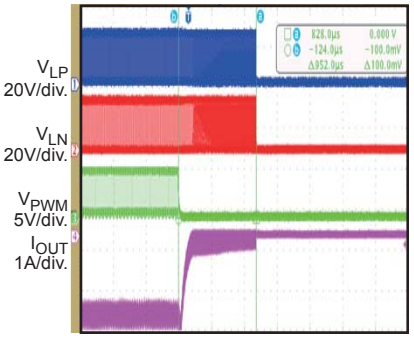
40ms/div.

Sleep Entry
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load



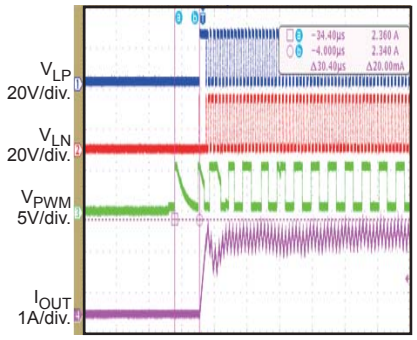
400μs/div.

Sleep Entry
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



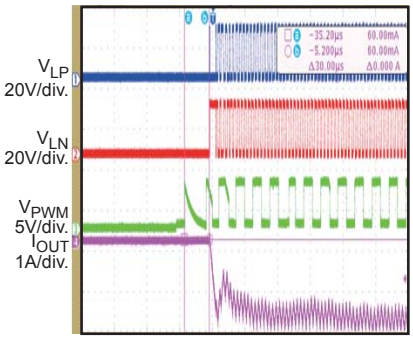
400μs/div.

Sleep Recovery
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load



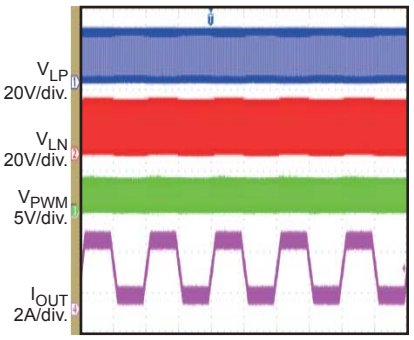
40μs/div.

Sleep Recovery
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



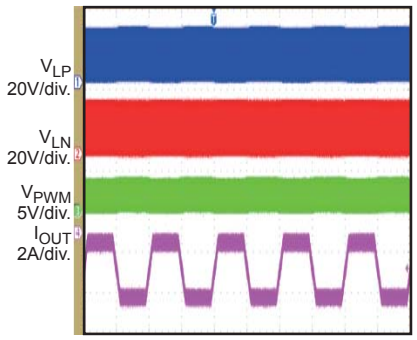
40μs/div.

Trapezoidal Wave
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load



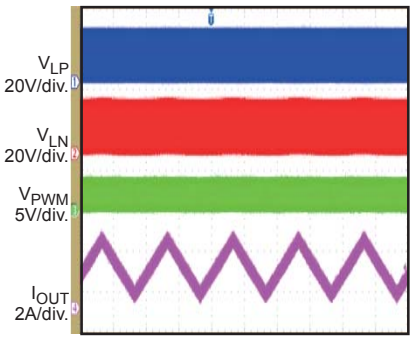
10ms/div.

Trapezoidal Wave
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



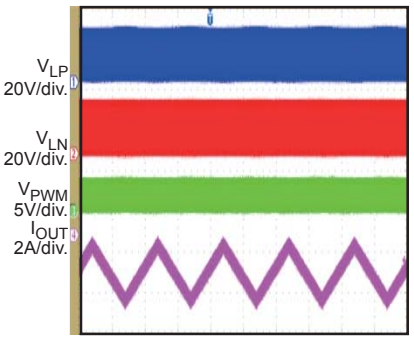
10ms/div.

Triangle Wave
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load



10ms/div.

Triangle Wave
V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



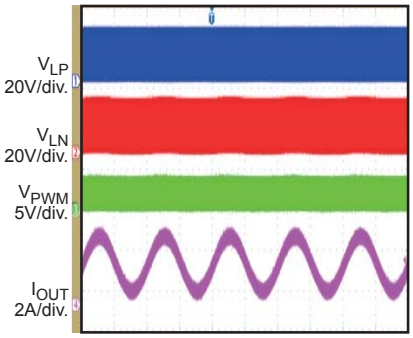
10ms/div.

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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

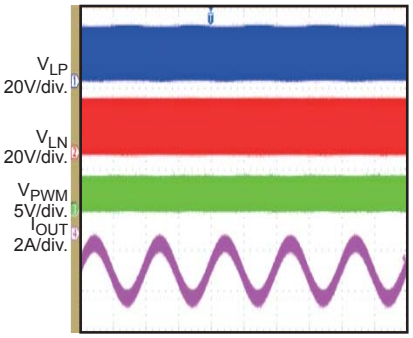
Sine Wave

V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = H, 1Ω+100μH Load



Sine Wave

V_{IN} = 24V, V_{EN} = 5V, Duty = 50%,
MODE = L, 1Ω+100μH Load



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PIN FUNCTIONS

Pin #	Name	Description
1	IFB	**Current sense signal feedback.** Connect IFB and ISEN together.
2, 11	VIN	**Input supply.**
3	LN	**Negative switching node of H-bridge.**
4	BSTN	**Bootstrap pin for LN high-side MOSFET gate driver.** Connect a capacitor between BSTN and LN.
5	EN	**IC enable.**
6, 7, 8	ISEN	**Current sense.** Connect a current sensing resistor between ISEN and power ground.
9	BSTP	**Bootstrap pin for LP high-side MOSFET gate driver.** Connect a capacitor between BSTP and LP.
10	LP	**Positive switching node of H-bridge.**
12	MODE	**Current polarity setting.** Assuming the current direction flowing from LP to LN is positive, drive MODE high to run the current from LP to LN; drive MODE low to run the current from LN to LP.
13	$\overline{FT}$	**Fault indication output.** $\overline{FT}$ is active low for fault conditions.
14	VCC	**5V LDO output for internal driver and logic.**
15	PWM	**PWM signal input for current dimming.** Apply a >20kHz PWM signal to PWM when used.
16	FREQ	**Switching frequency setting.** Connect a resistor from FREQ to GND.
17	ISET	**Full-scale current reference setting.** Connect a resistor to GND from ISET.
18	COMP	**Loop compensation setting.**
19	AGND	**Ground for internal logic.**

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BLOCK DIAGRAM

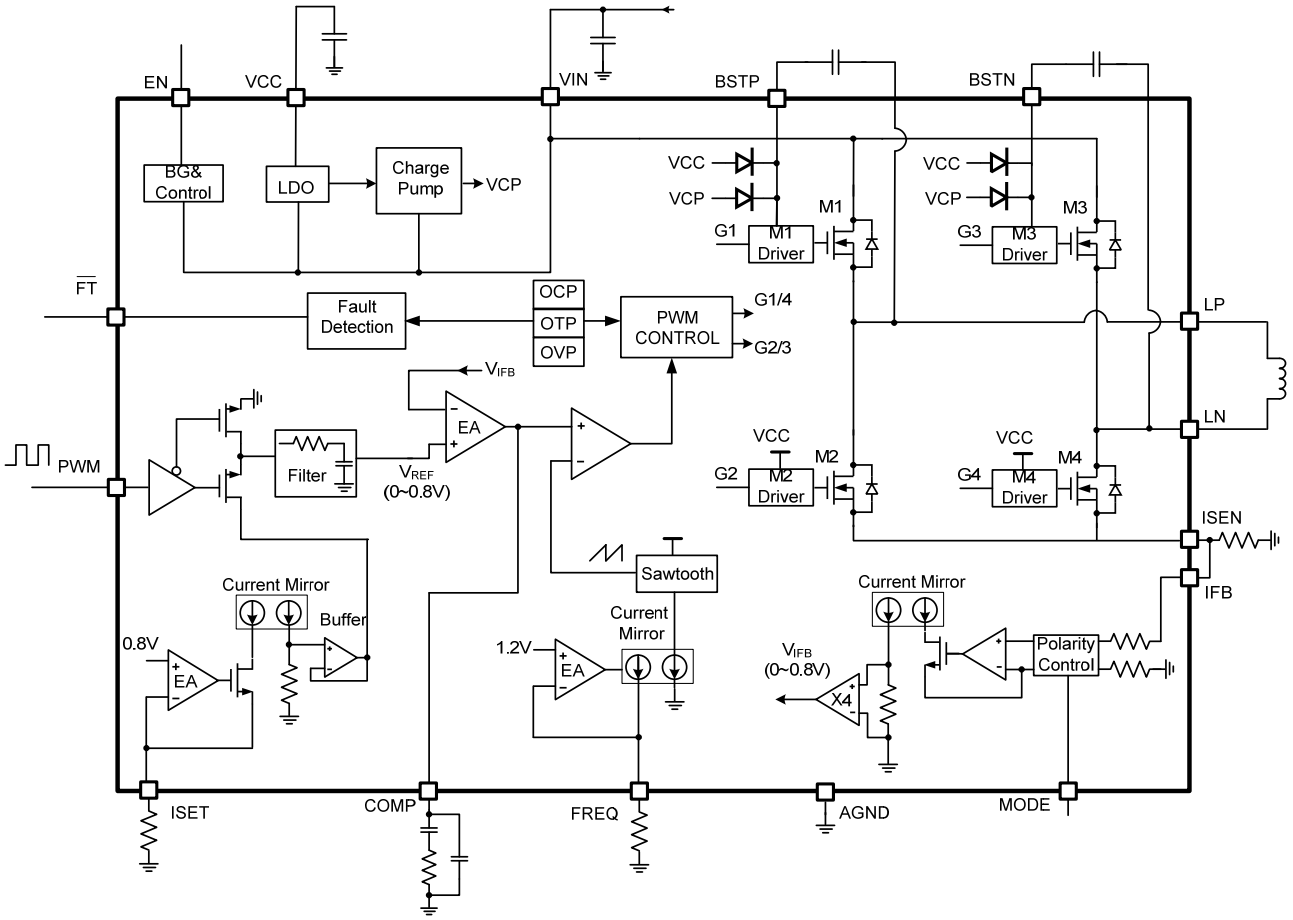


Figure 1: Functional Block Diagram

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OPERATION

The MP6519 is a current driver for applications that need to control the accurate load current and fast dynamic current response. The MP6519 works in step-down mode with four fully integrated MOSFET H-bridges to provide small size and high efficiency. The full-scale output current can be set by the external resistor, and the current polarity can be controlled by MODE to achieve a bidirectional current setting.

H-Bridge General Operation

The MP6519 works in a four-MOSFET H-bridge topology and uses pulse-width-modulation (PWM) with average current control to achieve a bidirectional current output and fast dynamic current response. The switching frequency is programmable from 30kHz to 300kHz.

In normal operation when enabled, the MOSFETs M1 and M4 turn on and off in the same sequence, and M2 and M3 turn on and off in the same sequence. M1/M4 and M2/M3 turn on an off in complementary operation with around 25ns of dead time to avoid device damage caused by a shoot-through. There is about 200ns of minimum on-time for all of the MOSFET switches (M1/M4 and M2/M3). Assuming the output current direction is set positive by pulling MODE high, the output current sensed by M2 and M4 is sent to the error amplifier negative input. By comparing the output current feedback signal with the current reference signal at the error amplifier positive node, the error amplifier outputs an appropriate voltage value which is compared with a sawtooth signal to provide a driver signal for M1/M4 and M2/M3. The device can enter four different modes described in the following sections to control the working sequence.

Shutdown Mode

The MP6519 goes into shutdown mode when pulling the EN signal low. In shutdown mode, all circuits and blocks are disabled, and the MP6519 consumes less than 1μA of shutdown current. There is about 150ns of deglitch time on EN to avoid a mistrigger.

Standby Mode

The MP6519 enters standby mode if either of following conditions are met:

- During start-up, the PWM signal on PWM is low while EN is high.
- After start-up in normal switching operation, the PWM signal keeps low for >1ms if EN is high.

In standby mode, the bandgap block and other control blocks begin working except for the gate drive block for the internal switching MOSFETs. This way, the device stops switching to reduce the quiescent current at no load. Meanwhile, standby mode can minimize the time that the output current tracks the reference signal of the PWM input, which comes after the EN signal. Since the MP6519 needs some time to establish the bandgap signal and other necessary control blocks, it is recommended that the PWM signal comes at least 300μs after the EN signal switches high.

Normal Switching Mode

If both the PWM and EN signals keep high, the MP6519 enters normal switching mode immediately. In this mode, the output feedback current closely follows the reference signal, which is received from the PWM input signal through an R-C filter (see the Current Feedback section on page 15 and the PWM Input Current Dimming section on page 14).

The H-bridge MOSFETs work in a fixed switching frequency (see the Switching Frequency Setting section on page 14). The output current polarity can be changed easily by pulling MODE high or low (see the following Current Polarity Mode section).

Current Polarity Mode

The current polarity is set by MODE. By pulling MODE high, the current is positive, and the current direction is from LP to LN. By pulling MODE low, the current is negative, and the current direction is from LN to LP. There is about 150ns of deglitch on MODE to avoid a mistrigger.

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Full-Scale Current Setting

The full-scale current reference value is set by connecting a resistor between ISET and GND. When I_{SET} is floating, the full-scale current reference voltage is set to the default 200mV. If a resistor is connected between I_{SET} and GND, the full-scale current reference voltage can be reduced below 200mV to reduce power loss on the feedback resistor. The IC needs about 0.3ms to detect whether a resistor is available or not on ISET when the IC starts up for the first time. During this time, the IC is not switching. The relation of the full-scale current reference voltage and R_{ISET} is shown in Equation (1):

$$V_{REF_FULL} = 0.2^* \frac{40}{R_{ISET}(k\Omega)} \quad (1)$$

For example, if R_{ISET} is 80kΩ, the reference voltage is 100mV. For better accuracy, 40kΩ to 80kΩ is recommended to achieve a 200mV to 100mV current reference voltage.

Start-Up Sequence

The IC needs about 0.3ms to detect whether a resistor is available or not on ISET when the IC starts up for the first time. During this time, the IC is not switching. It is recommended to apply a PWM signal at least 0.3ms after the EN signal (see Figure 2 and Figure 3).

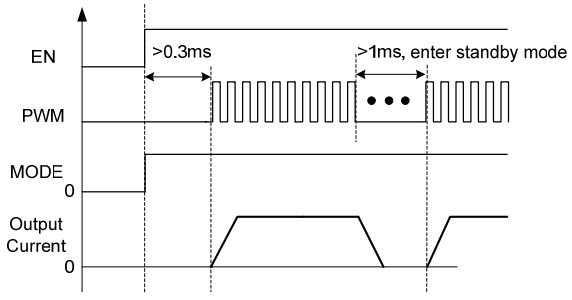


Figure 2: Positive Output Current Mode

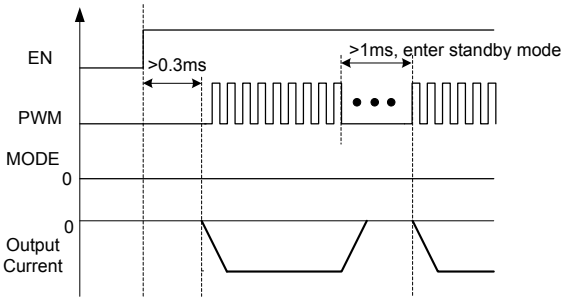


Figure 3: Negative Output Current Mode

Switching Frequency Setting

The H-bridge MOSFET switching frequency is set by FREQ by connecting a resistor between FREQ and GND. With a proper resistor value, the switching frequency can be set between 30kHz and 300kHz. A higher switching frequency leads to a smaller current ripple, but the MOSFET switching loss is larger. Therefore, a trade-off is needed for the design. The switching frequency setting formula is shown in Equation (2):

$$f_{FREQ} = \frac{22500}{R_{FREQ}(k\Omega)} \quad (2)$$

PWM Input Current Dimming

If the full-scale output current reference is set, the actual output current reference sent to the error amplifier can be further controlled by applying a PWM input signal to PWM. This way, V_{REF_FULL} is chopped by the PWM input signal, and the current reference voltage is received from this chopped PWM voltage through the internal low-pass filter. For a smaller output current reference ripple, the input frequency of PWM is recommended to be 20kHz to 100kHz. Considering the full-scale reference, the relationship between the actual output current reference and duty cycle of the PWM input (D_{PWM}) is shown in Equation (3):

$$V_{REF_FB} = 0.2^* \frac{40}{R_{ISET}(k\Omega)} * D_{PWM} \quad (3)$$

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Current Feedback

The current flowing through the load is sensed through a resistor connected between IFB and GND. This sensing voltage on IFB is sent to the feedback block circuit and used to generate the average feedback voltage (V_{IFB}), which is equal to the average output current multiplied by the sensing resistor value (R_{IFB}). V_{IFB} is sent to the error amplifier negative node and compared with the output current reference voltage on the error amplifier positive node. The output of the error amplifier is COMP. The COMP voltage (V_{COMP}) is used to generate the internal MOSFET switch on and off times.

The simple block is shown in Figure 4.

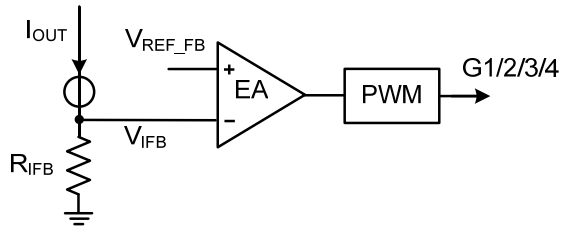


Figure 4: Current Feedback Loop

VCC LDO Regulator

The IC employs an LDO regulator to provide a constant voltage (5V) at VCC. The VCC voltage is used for the internal power supply of the logic circuit and driver circuit. When the input voltage is high enough (larger than 5.2V), the VCC output is 5V. When the input voltage drops below 5V, the VCC voltage drops together with the input voltage. The dropout voltage is around 100mV. If the VCC voltage drops below 2.15V, the IC triggers a power reset sequence and shuts down. The IC resumes normal operation when VCC is higher than 2.3V.

High-Side MOSFET Driver

The high-side MOSFETs of M1 and M3 are N-channel MOSFETs. When M1 and M3 turn on, a bootstrap supply voltage across BSTP and BSTN is needed. The bootstrap voltage is generated by a combination of the internal charge pump and a 5V VCC. This allows the IC to work in 100% duty cycle to provide enough driver voltage for the high-side MOSFETs (M1 and M3).

Over-Current Protection (OCP)

To provide robust protection during an over-current event, the IC uses a two-level protection mode.

If the current flowing through the MOSFETs is larger than 150% of the full-scale setting value during two consecutive switching cycles, the IC stops switching and triggers a power reset sequence to restart after 1ms.

If the current flowing through the MOSFETs is larger than 200% of the full-scale setting value, the IC will latch off. If the high-side MOSFET hits over-current, the high-side MOSFET is turned off immediately and the Fault pin is driven low. At the same time, the two low-side MOSFETs are turned on for several milliseconds and then the two low-side MOSFETs are turned off and IC latches off. The reverse will happen if the low-side MOSFET hits over-current where the low-side MOSFET is turned off immediately and the Fault pin is driven low. And at the same time the high-side MOSFETs are turned on for several milliseconds and then the high-side MOSFETs are turned off and IC latches off.

Input Over-Voltage Protection (OVP)

During operation, the energy stored in the load current is delivered to the input side during the free-wheeling time. If the input voltage and output current are high enough, the energy sent back to the input side causes the input voltage to rise up. To avoid IC damage due to a high voltage spike, the IC employs input voltage protection. If the input voltage is higher than the input over-voltage threshold for four consecutive switching cycles, the IC stops switching and latches off immediately.

Junction Over-Temperature Protection (OTP)

If the IC junction temperature (T_J) is higher than 150°C, the IC stops switching and resumes normal operation when T_J drops below 130°C.

Fault Indication Output ($\overline{FT}$)

In normal operation, $\overline{FT}$ is a high-impedance open drain. If any fault occurs during operation, $\overline{FT}$ is pulled low to indicate the fault condition for the external system. Recycle the input power or toggle the EN signal to remove the fault latch condition.

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Enable/Disable (EN)

To enable the IC, a logic-high signal needs to be applied to EN, and the high-level signal time needs to be higher than about 10μs. To shut down the IC, pull EN to logic low, and the low-level signal needs to higher than 100ns.

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APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. A higher value capacitor is helpful for reducing input voltage ripple and noise. For most applications, two 22μF ceramic capacitors in parallel are sufficient. It is recommended to connect one capacitor on each VIN pin.

Setting the Full-Scale Output Current

If a resistor is connected between I_{SET} and GND, the full-scale output current reference (V_{REF_FULL}) can be calculated with Equation (4):

$$I_{OUT} = 0.2 * \frac{40}{R_{ISET}(k\Omega)} * \frac{1}{R_{IFB}(\Omega)} \quad (4)$$

If ISET is left floating, the current setting formula is as shown in Equation (5):

$$I_{OUT} = \frac{0.2}{R_{IFB}(\Omega)} \quad (5)$$

For example, if R_{ISET} is 80kΩ, then the reference voltage is 100mV. For better accuracy, 40kΩ to 80kΩ is recommended to achieve a 200mV to 100mV current reference voltage.

Setting the Feedback Resistor

The power loss of the sensing resistor can be calculated with Equation (6):

$$P_{LOSS_RIFB} = \frac{V_{REF_FULL}^2}{R_{IFB}(\Omega)} \quad (6)$$

To guarantee a current reference, the nominated power rating of the sensing resistor is recommended to be twice the calculated power loss with at least a 1% accuracy resistor.

Setting the Switching Frequency

A higher switching frequency leads to a smaller current ripple but a higher switching loss of the MOSFETs. Therefore, a trade-off is required for the design. The switching frequency setting can be calculated with Equation (7):

$$f_{FREQ} = \frac{22500}{R_{FREQ}(k\Omega)} \quad (7)$$

Since the power loss of this resistor is small, a resistor size 0603 or 0402 is sufficient.

Selecting the Compensation Loop

The loop compensation components can be used to make the closed loop stable and achieve a better transient response (see Figure 5).

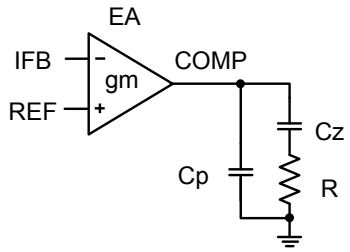


Figure 5: Compensation Loop

The transfer function of the loop compensation from the EA input to the EA output can be calculated with Equation (8):

$$G_c(s) = \frac{g_m}{(C_z + C_p)s} \frac{(1 + sRC_z)}{(1 + sR\frac{C_zC_p}{C_z + C_p})} \quad (8)$$

Where g_m is the EA transconductance value.

The transfer function zero point is made up from R and C_z. The pole point is made up from R and the value of C_z in parallel with C_p.

Usually, for an inductive load with resistance, the compensation zero can be set as the load pole made of the load inductance (L) and its resistance value. The compensation pole point is usually set around the switching frequency point to eliminate high-frequency noise. After the zero and pole point of the compensation is fixed, R can be used to increase the loop bandwidth. 1/10 to 1/5 of the switching frequency can be set as the close-loop bandwidth to achieve a good system response.

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, follow the guidelines below.

1. Place the input capacitor close to VIN.
2. Use a wider copper for input, output, and the GND connecting wire to improve thermal performance.
3. Place as many GND vias near the output and input capacitor as possible to improve thermal performance.
4. Keep the IFB feedback signal far away from noise sources.

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TYPICAL APPLICATION CIRCUIT

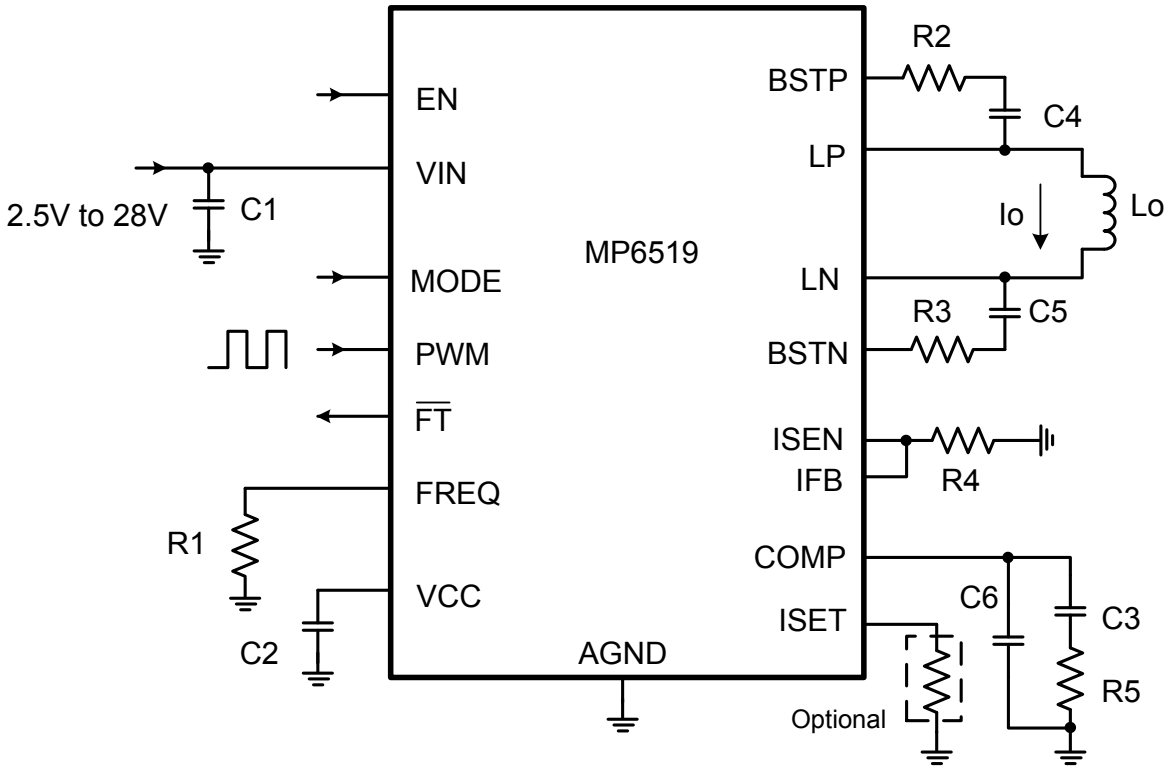
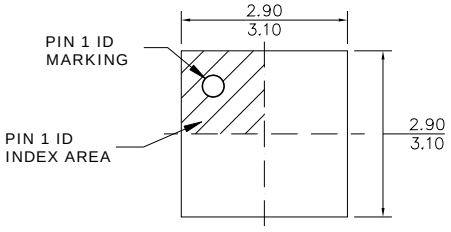


Figure 6: Typical Application

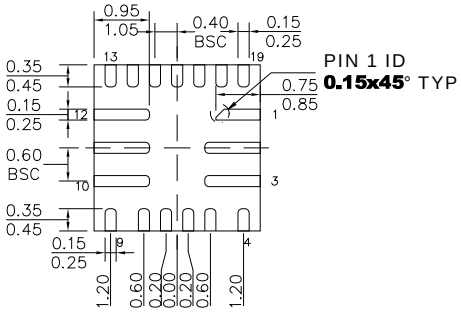
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PACKAGE INFORMATION

QFN-19 (3mmx3mm)



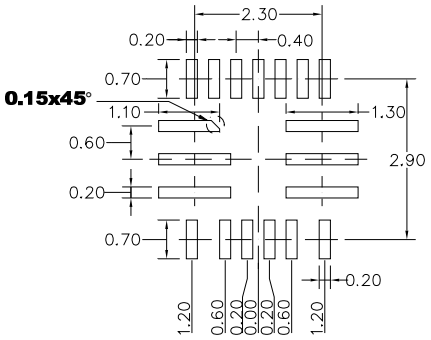
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN2,3,10,11 AND 12 HAVE THE SAME SHAPE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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